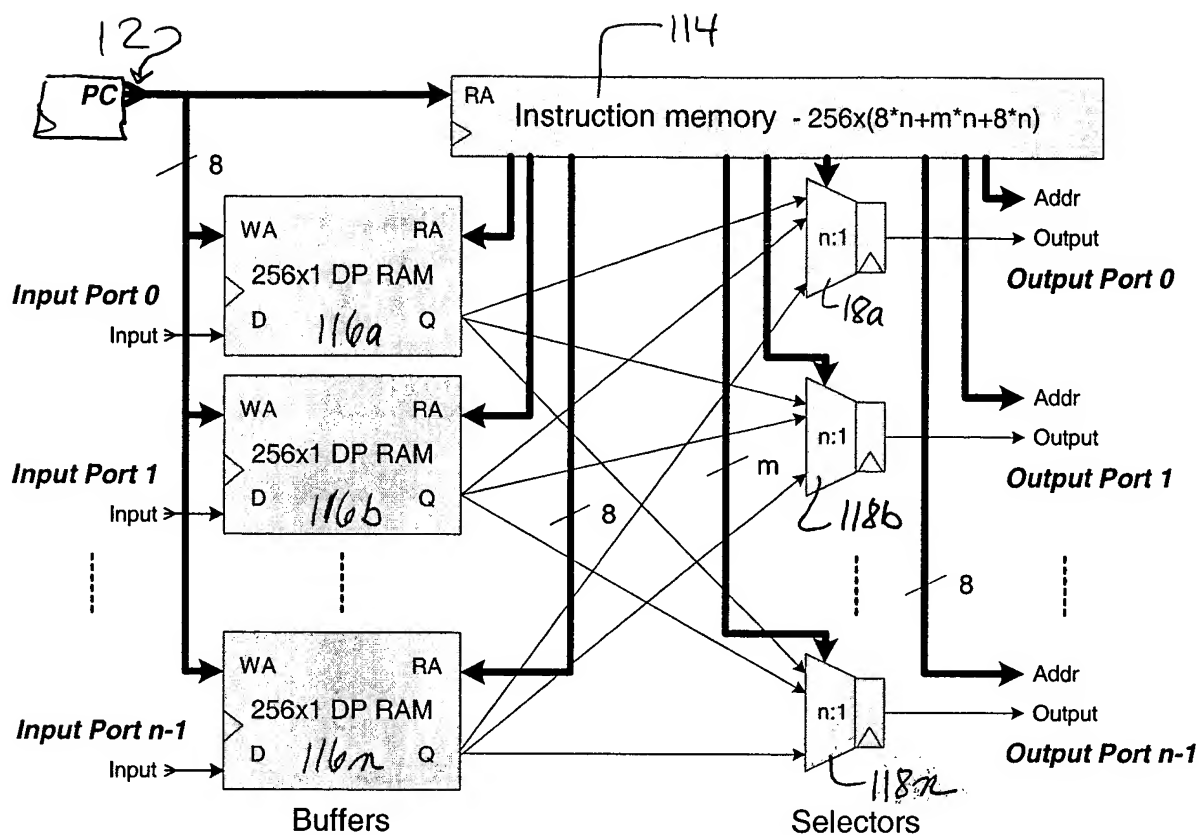


**Fig. 1: Logic Processor for programming into FPGAs**  
 (All memories and registers are synchronously clocked by the common system clock.)

Fig. 1



100 v

Fig. 2

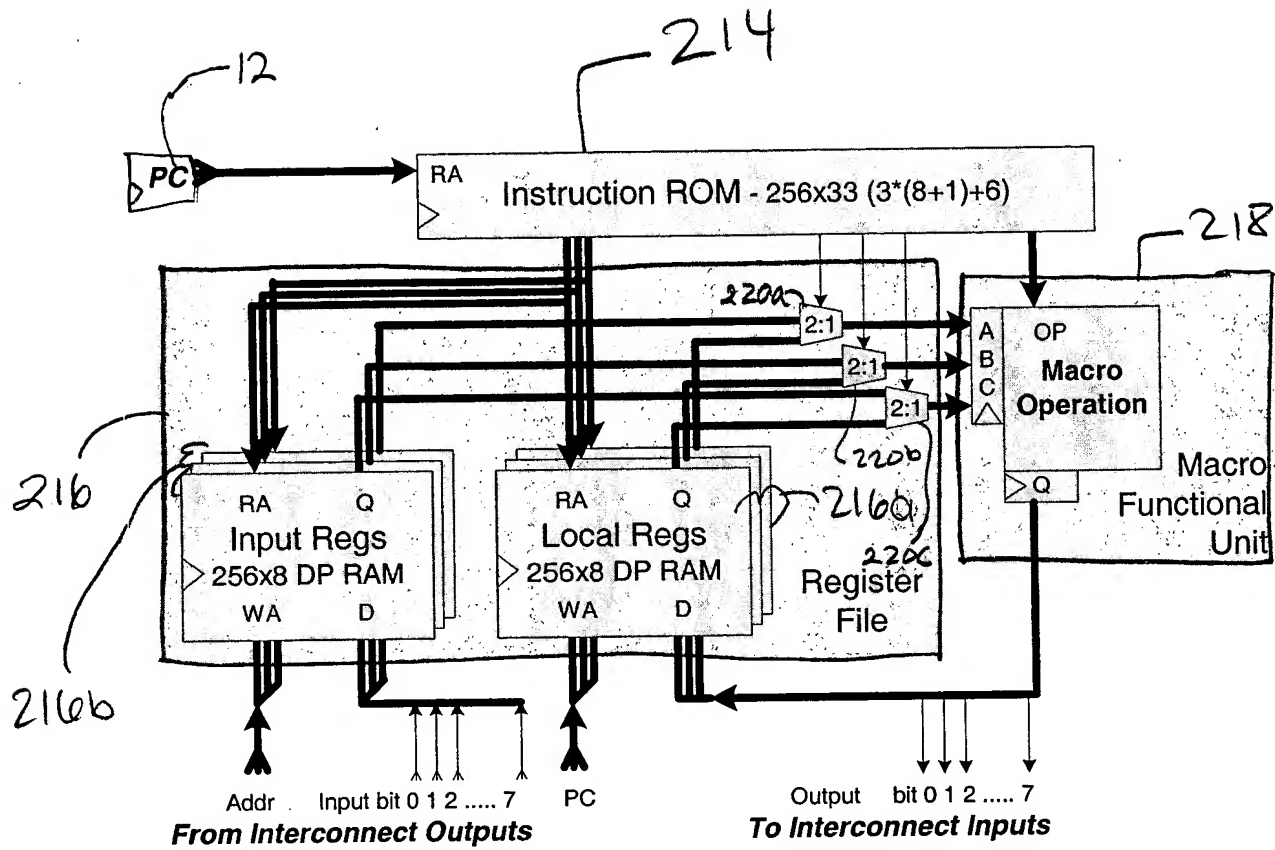


Fig. 3: Macro Processor

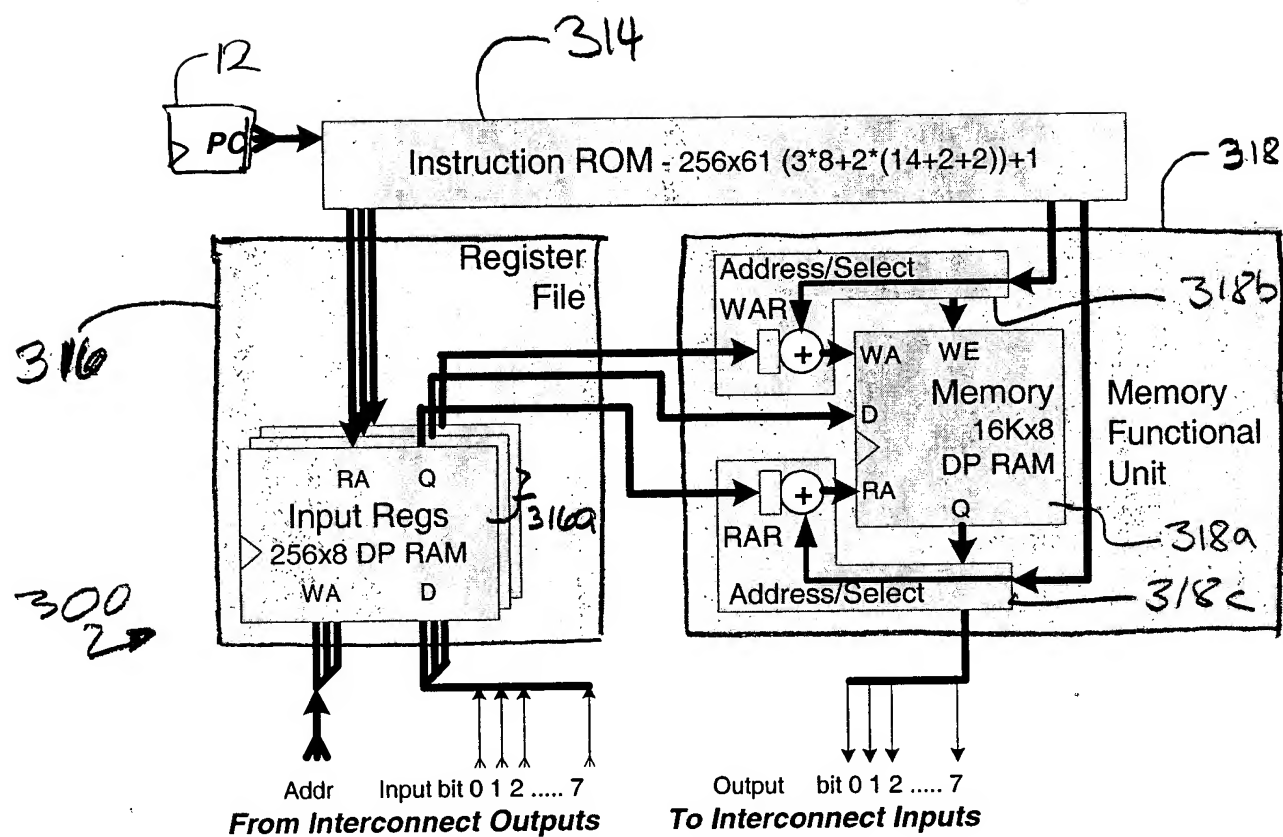


Fig. 4: Memory Processor

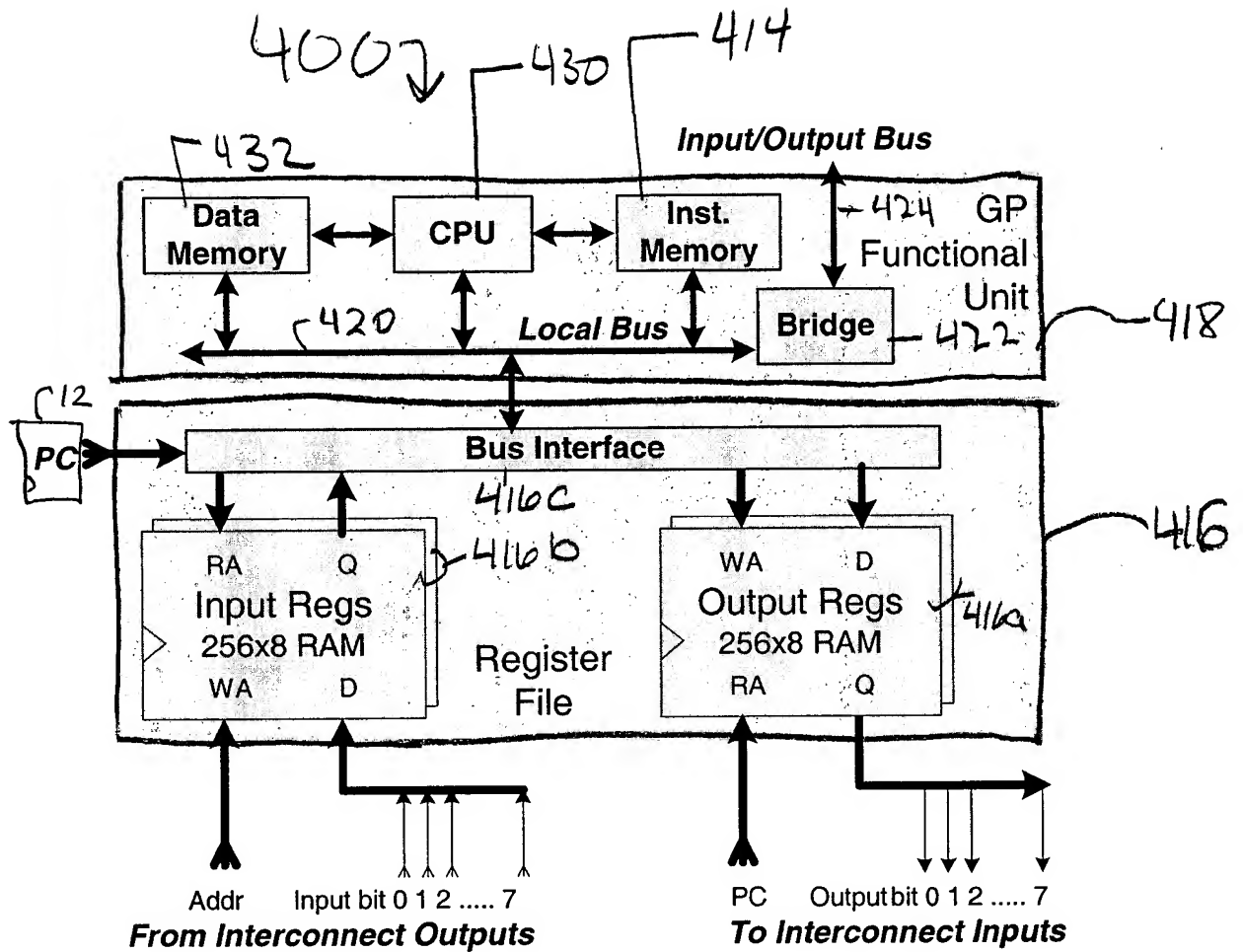
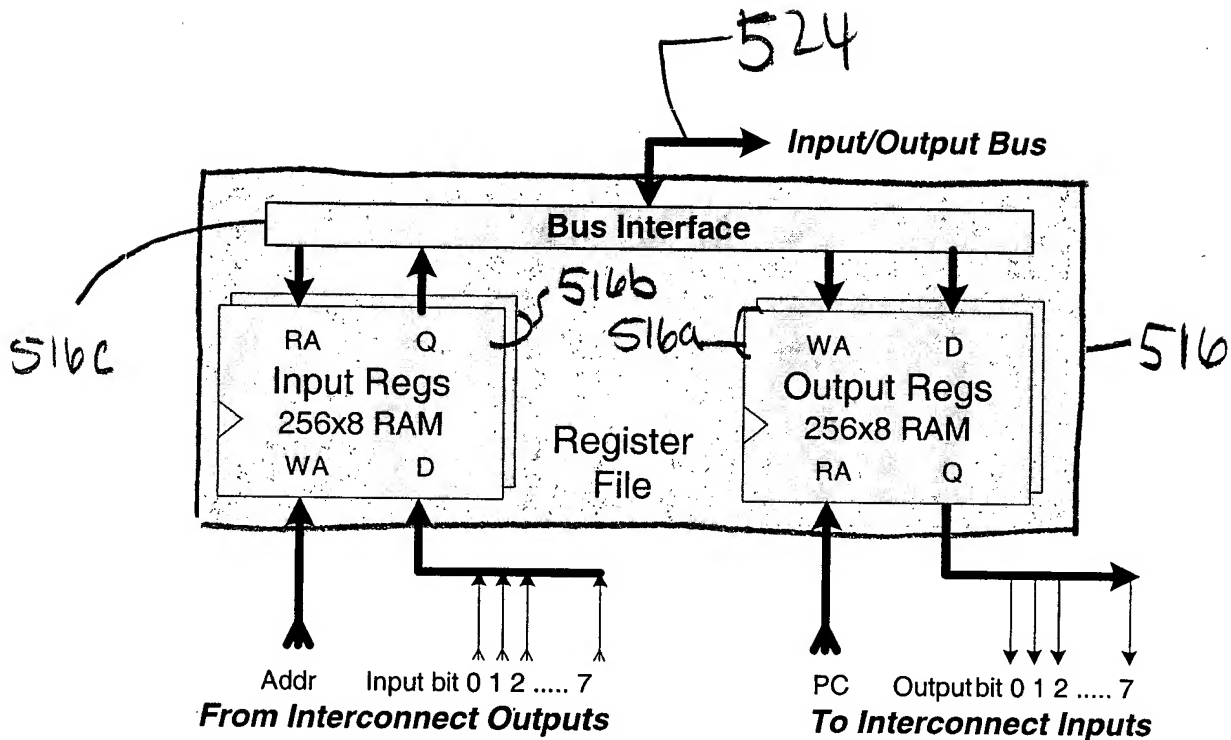
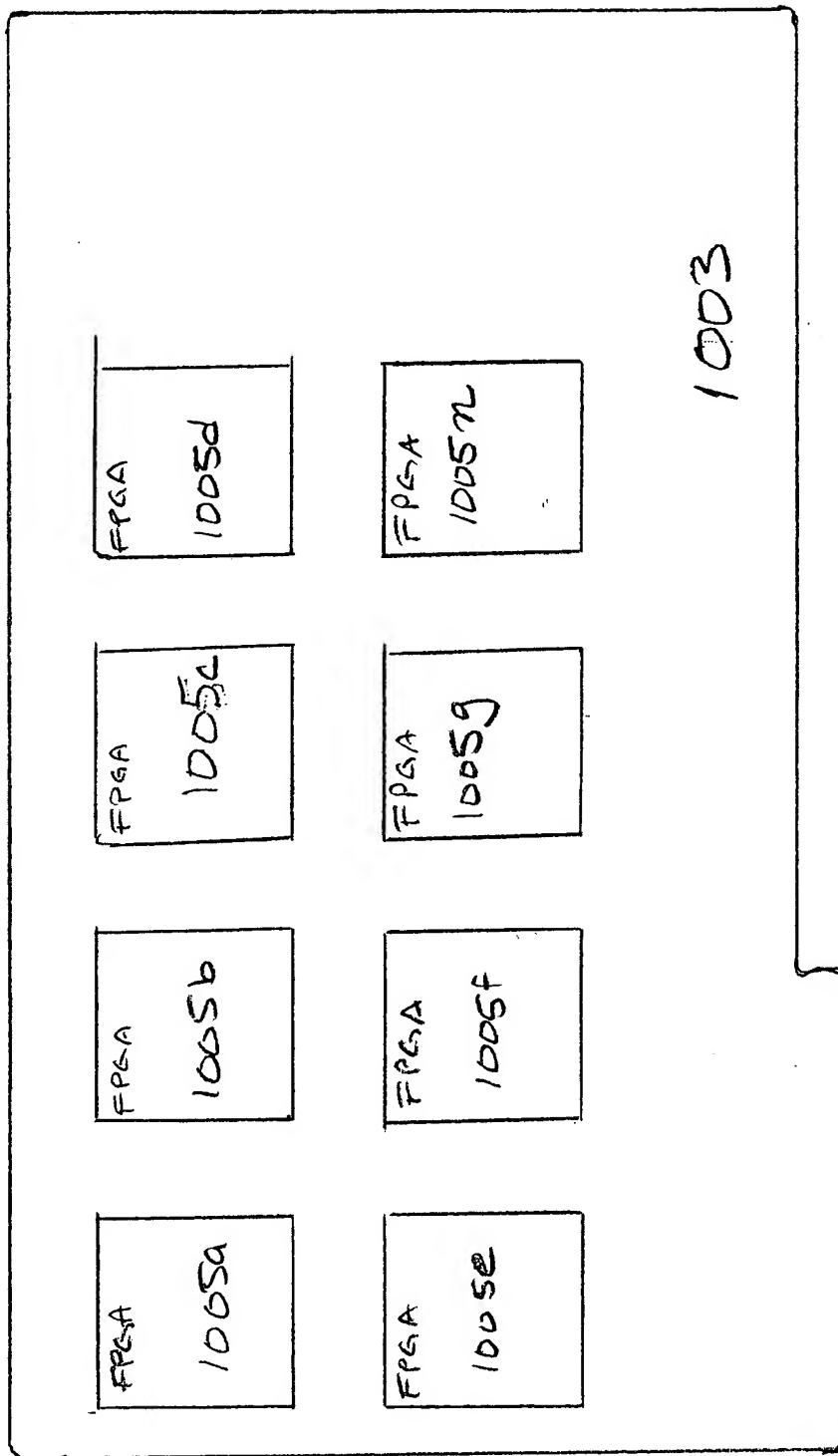


Fig. 5: General Purpose Processor



500

Fig. 6: Interface Unit



1000 ↗

Fig. 7